PATENTS
112025-0166
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REMARKS

This Amendment after FINAL Rejection is filed in response to the Office Action mailed on December 3, 2003. All objections and rejections are respectfully traversed.

Claims 1-3, 5-7, 9-11, 13-17 are in the case.

No claims were added or amended.

Applicant respectfully requests that the present Amendment After FINAL Rejection be entered and considered. Applicant has already filed one CPA on February 6, 2003, and the present Amendment After FINAL Rejection mainly responds again to concerns expressed earlier by the Examiner concerning issues under 35 U.S.C. § 112, first paragraph.

At Paragraph 2 of the Office Action it was pointed out that there was a typographical error in use of reference numerals "92" and "93". Amendment of the specification is believed to satisfy this objection.

At Paragraphs 3, 3.1, 3.2 claims 1-3, 5-7, 9-11, and 13-17 were rejected under 35 U.S.C. § 112, first paragraph. At Paragraph 3.2, bottom of page 3 of the Office Action, it is stated:

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"While the Specification at page 16 lines 5-11 appears to discuss empirically determined rule for selecting a portion of a circuit for simulation using physical characteristics, no flowcharts or text in the Specification appears to describe:

(1) how to interconnect the computer components and program them to pass the data necessary to determine the timing based on physical characteristics or hierarchical analysis; or

(2) how to combine the physically accurate description of the timing of the first system portion with the approximate mathematical model of the timing of a remaining system portion."

Further, at the bottom of page 4 of the Office Action, it is further stated:

"Taken as a whole, only with undue experimentation could one reasonably skilled in the art make an/or use the invention described in the specification."

Applicant respectfully urges that the level of skill of a person practicing the present invention is set by reference to Prior Art Fig. 6.

Applicant respectfully points out that Prior Art Fig. 6 shows computer modeling of an electronic system (including a computer system) using hierarchical analysis, where the hierarchical analysis function (HA function) is computed at block 28. In contrast, Applicants' claimed novel invention is shown in Fig. 1, where Applicants' novel use of the "Composite Modeling Engine" at block 30 is shown.

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Applicant respectfully urges that a person of ordinary skill in the art who is skilled in programming the computer program represented by Prior Art Fig. 6 would be able to add Applicants' claimed new "Composite Modeling Engine" 30, by following the instructions set out by Applicant in the present Specification, without undue experimentation.

At Paragraphs 4, 4.1, 4.2, 4.3 Applicant's arguments in the last Office are summarized by the Examiner. Then, at Paragraph 5.1 the Examiner responds to Applicant's arguments, as summarized.

Particularly, at Paragraph 5.1 it is stated:

> Regarding the rejections made under Section 112, the Specification and drawings do not appear to describe how to make the claimed invention. Applicants' argument that the Specification at page 8 line 21 to page 9 line 16 teaches how to interconnect the computer components appears incorrect. The quoted text from the Specification describes "module 65."
>
> However, module 65 does not appear to be part of the system that performs the simulation; instead, module 65 appears to be part of the system to be simulated. See Figs. 1 and 3 and the Specification at page 8 lines 1-20, describing the "proposed design 100" that includes "module 65."
>
> As described above, the Specification does not appear to describe how to make or program the computer system to combine the separate "physically-accurate description" and "approximate model" into a timing simulation. The fact that hierarchical analysis is well-known, as demonstrated by Kukimoto et al., does not indicate that one skilled in the art would be able to use Applicants' Specification to make a simulation that split a system into portions with one portion simulating timing based on a physically-accurate description and the other portion simulating timing using hierarchical analysis.

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Applicant notes that the suggestions in MPEP 2106.02 that flow charts be used to represent a new computer program are fully met by Applicants' figures, Fig. 1 -through- Fig. 6.

Applicants respectfully urges that their figures, Fig. 1 - Fig. 6, are flow charts of a computer program. The blocks represent computational sections of the program, and the arrows represent information flow within the computer program. In particular, Fig 6 is a flow chart representing Prior Art computer programs which simply do hierarchical analysis using "HA Modeling Engine" 28. In sharp contrast, Fig. 1 is a flow chart of Applicants' claimed novel invention in which the computer program uses Applicants' novel "Composite Modeling Engine" 30.

Further, Fig. 4 is a flow chart of a Prior Art computer program which uses hierarchical analysis at block 82 which estimates the HA function of part (parts A, B, X, Y) of the electronic system being simulated, and estimates another HA function (part Net) of estimated model) at block 84, and which estimates still another HA (parts C, D, and Z) function at block 86.

In sharp contrast, Fig. 5 is a flow chart showing the use of hierarchical analysis at block 90 to estimate part (parts A, B, X) of the electronic system being simulated, and

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then at blocks 93 (part Y), 94 (part Net), and 96 (part Z) uses a physically accurate description of selected portions of the electronic system being simulated. Then at block 92 still further parts (parts C, D) of the electronic system are estimated using hierarchical analysis by computation of an HA function of parts C and D.

A factual basis for Applicant's assertion that Applicants' Fig. 1 -through- Fig. 6 represent flow charts of computer programs, as suggested by MPEP 2106.02, is found in the Specification by reference to the blocks of the figures as "functional blocks", especially in the Brief Descriptions of the Drawings section on Pages 6-7. Each of the drawings is referred to as a "functional block diagram", or a "block diagram", with arrows indicating flow of information between the functional blocks.

Further, Applicant notes that the electronic system which is being simulated is described in the Specification at page 4 lines 7-13 in the Background section as the electronic system set out in the copending patent applications (some of which are issued as U. S. Patents, see below) incorporated by reference at pages 1-2 of the Specification as:

> Unfortunately, in practice, it is often difficult or impossible to employ this conventional technique to simulate the operation of certain highly complex parallel processor designs (such as those described in the aforesaid copending applications). This is because, in practice, the amount of computer processing time (hereinafter termed "processing overhead") required to accurately simulate the operation of such highly complex designs using such physical characteristics often is extremely large, and in extreme cases, can be prohibitive.

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Also, at page 8 lines 10-20 in the Detailed Description section of the Specification reference is made to the electronic system being modeled as:

> By way of example, for purposes of illustrating the operation of the system 10, and with reference being made to Figure 3, the proposed design 100 may be part of a parallel processor system of the type described in the aforesaid copending patent applications, and may include a plurality of functional modules or blocks (i.e., function blocks A, B, C, D, X, Y, and Z) 60, 62, 64, 66, 72, 74, 76 that interact with each other and generate outputs 78 based upon inputs 50, 80 and timing (i.e., clock) signals CLK.

Accordingly, Applicant respectfully urges that the answer to the inquiry by the Examiner concerning whether the drawings (including "module 65") of the present Application for U. S. Patent represent the system to be simulated or represent a flow chart of the simulation system are answered by the quotations above: at page 4 "conventional technique to simulate the operation of certain highly complex parallel processor designs (such as those described in the aforesaid copending applications)"; and at page 8 "By way of example, for purposes of illustrating the operation of the system 10, and with reference being made to Figure 3, the proposed design 100 may be part of a parallel processor system of the type described in the aforesaid copending patent applications"; and the answer is that the present drawings, Fig. 1 - Fig. 6, are block drawings of flow charts of the claimed simulation system.

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The Examiner particularly raised a question at Page 6 of the Office Action, second paragraph of section 5.1, as to whether "module 65" is part of the electronic system to be simulated, or is part of the simulation process.

Applicant respectfully urges that all modules in the present figures Fig. 1 - Fig. 6 are functional blocks in flow charts of the simulation process, including "module 65".

Applicant further notes that the language used in the present Application for U. S. Patent directly ties the present flow charts and functional blocks to the hardware being represented in the simulation by the language used in the above quotations, particularly at page 8 lines 1-20 of the specification. However, it is clear from the totality of expression that electronic systems as described in the "copending applications" are being simulated by the present simulation system.

As an aid to the Examiner, the Copending Patent Applications mentioned in the present Specification at Pages 1-2 which have issued, are listed by Issued Patent Number hereinbelow, and a copy of each issued co-pending patent is enclosed herewith:

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U. S. Patent Number	Date Issued
6,153,108	Jan. 28, 2003
6,385,747	May 7, 2002
6,195,739	Feb. 27, 2001
6,173,386	Jan. 9, 2001
6,119,215	Sept. 12, 2000
6,101,599	August 8, 2000

Applicant respectfully notes that each of these issued patents are referred to in the Specification using the language:

> "Each of the aforesaid copending applications is assigned to the Assignee of the subject application, and is incorporated herein by reference in its entirety." (Specification, page 2 lines 7-8)

Accordingly, Applicant respectfully notes that the copending patent applications, and the patents which issued from them, are both referred to as an example of an electronic system which is to be simulated, and their disclosures are incorporated into the present U. S. Patent Application by reference. It is therefore clear that the present Application is for a simulation system, and as examples, the electronic systems mentioned in the issued U. S. Patents may be simulated by the presently claimed invention.

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Applicant respectfully urges that all requirements of 35 U. S. C. § 112 are met by the present disclosure, especially the requirements of 35 U. S. C. § 112, first paragraph, which states:

> "The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention."

Applicant respectfully urges that "a person skilled in the art to which it pertains" is a person who makes and uses simulation systems such as shown in Prior Art Fig. 6, and Prior Art Fig. 4, and that such a person can follow Applicants' instructions to add Applicants' new "Composite Modeling Engine" 30 as shown in Fig. 1, without resort to undue experimentation. Further, persons who are skilled in "the art to which it pertains" include persons who design complicated electronic systems such as the computer systems disclosed in the copending patent applications referred to at pages 1-2 of the Specification. Persons, sufficiently skilled in the art to understand and work with the cited Prior Art and the electronic computer systems described in the copending patent applications, are surely sufficiently skilled in the art to follow Applicant's instructions to make and use Applicants' claimed novel invention.

All independent claims are believed to be in condition for allowance.

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All dependent claims are believed to be dependent from allowable independent claims, and therefore in condition for allowance.

Favorable action is respectfully solicited.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

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